UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/669,354	09/26/2000	Hisanobu Ishiyama	81751.0009	4577

26021 7590 02/24/2003

HOGAN & HARTSON L.L.P.
500 S. GRAND AVENUE
SUITE 1900
LOS ANGELES, CA 90071-2611

EXAMINER	
NGUYEN, HAU H	
ART UNIT	**PAPER NUMBER**
2676	

DATE MAILED: 02/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/669,354	ISHIYAMA, HISANOBU	
	Examiner	Art Unit	
	Hau H Nguyen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Response to Argument

1. The amendment filed on December 10, 2002 is fully considered, but is not persuasive. In the remarks section, Applicant argues that Strobel et al. does not teach that "each of the master IC and the at least one slave IC has an input terminal for receiving the display control signal output from the display control signal generation section of the master IC through an external wiring". The examiner agrees with Applicant that SIN is the input data, not the control signal. However, Strobel et al. do teach a control signal from an external MPU through terminals C1 and C2. According to Strobel et al., control signals are applied from outside to the internal circuit blocks via the inputs C1 and C2 (col. 14, lines 10-11). As shown in Fig. 5, terminals C1 and C2 which permit the operating mode of the IC to be selected (it is noted that 'operating mode control BAS itself is externally controlled', col. 8, lines 46-48). If a plurality of ICs are to be connected to form a chain, C1 and C2 of the master are connected to the controlling processor, cf. also FIG. 5 (control signal is enabled for master IC). On the other hand, in all the slaves C1 is constantly applied to high level and all the C2 terminals are directly connected to the C2 terminal of the master, cf. FIG. 5 (control signal is disabled for slave IC) (col. 12, lines 37-42). For example,

C1=C2=0: the shift register SR1 is loaded out of the text memory TS;

C1=0; C2=1: the data are loaded by the input SIN into the shift register,

C1=1; C2=0: the data are loaded by the input SIN directly into the shift register SR1;

C1=C2=1: the input SIN is blocked (col. 12, lines 44-58). Thus, when C1 = C2 = 1, the display control signal is delayed.

DETAILED ACTION

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1-7, 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bird et al. (U.S. Patent No. 5,852,425) further in view of Strobel et al. (US Patent No. 5,420,600).

Referring to claims 1, 4, 5, and 7, Bird et al. an active matrix display device comprising sets of row and column conductors, an array of display elements each comprising first and second electrodes with electro-optical material therebetween, the first electrodes being connected to the drain of a respective TFT whose source and gate are connected respectively to a column and a row conductor, and a drive circuit for driving the display elements comprising a scan drive circuit for applying selection signals to the row conductors and a data signal drive circuit connected to the column conductors which includes means for providing time dependent pulse signals representing video information, which is characterized in that the data signal drive circuit is arranged to supply the time dependent pulse signals to the column conductors and includes means for biasing the TFTs during the application thereto of a selection signal such that the TFTs act as current sources (see col. 3, lines 33-49). Thus, Bird et al. teach all the limitations of claim 1, 4, 5, and 7 except for the driving circuits having a master IC and at least one slave IC, an internal delay circuit to delay the control signal, and each of the master IC and the at least one

slave IC has an input terminal for receiving the display control signal output from the display control signal generation section of the master IC through an external wiring.

However, Strobel et al. teach an IC apparatus for providing a timed drive of a display matrix comprising plurality of ICs (IC1... ICn) forming a chain by their shift registers being connected in series so that the short codes supplied by the microprocessor μP are supplied in each case to the signal input SIN of the shift register of the first IC IC1, and via the signal output SOUT of this shift register also to the signal input SIN of the following ICs...ICn (see Fig. 2, and col. 7, lns 50-58). Figure 5 shows a circuit according to FIG. 2 is to be built up with n=2 ICs wherein a chain of two IC examples, a master corresponding to the first IC and of a slave corresponding to the second IC. Strobel et al. further teach a control signal from an external MPU through terminals C1 and C2. According to Strobel et al., control signals are applied from outside to the internal circuit blocks via the inputs C1 and C2 (col. 14, lines 10-11). As shown in Fig. 5, terminals C1 and C2 which permit the operating mode of the IC to be selected (it is noted that 'operating mode control BAS itself is externally controlled', col. 8, lines 46-48). If a plurality of ICs are to be connected to form a chain, C1 and C2 of the master are connected to the controlling processor (col. 12, lines 35-39). For example, C1=C2=0: the shift register SR1 is loaded out of the text memory TS;

C1=0; C2=1: the data are loaded by the input SIN into the shift register,

C1=1; C2=0: the data are loaded by the input SIN directly into the shift register SR1;

C1=C2=1: the input SIN is blocked (col. 12, lines 44-58). Thus, when C1 = C2 = 1, the display control signal is delayed.

Therefore, it would have been obvious to one of ordinary skills in the art to utilize the driving circuit having master/slave IC structure as taught by Strobe et al. in combination with the active matrix display device as taught by Bird et al. in order to obtain an operationally reliable, sturdy construction of the output register to be used, and reduce the flickering of the text during a change of the text to be displayed (see col. 6, lns 62-68 of Strobel et al.).

In regard to claims 2 and 16, as applied to claims 1 and 4 above, Bird et al. teach all the limitations of claims 2 and 16, except for each of the master IC and the at least one slave IC comprising a display memory, an a display address circuit. However, Strobel et al. teach each IC containing a read-only memory, which stores the bits required for the different displays and loaded into the shift registers of further IC/ICs and which transmits the relevant bits to the shift register of this IC when a relevant address or start address is called up, during operation only the read-only memory of the first IC of the chain, but not the read-only memory of the next, further IC/ICs of the chain, transmitting to the separate shift register of this first IC bits to the shift register of the next, further IC_x and during operation the shift register or registers of the further IC/ICs of the chain being loaded by the shift register of the respective preceding IC of the chain (col. 5, lns 9-56, Strobel et al.).

Therefore, it would have been obvious to one of ordinary skills in the art to utilize the driving circuit having master/slave IC structure as taught by Strobe et al. in combination with the active matrix display device as taught by Bird et al. in order to obtain an operationally reliable, sturdy construction of the output register to be used, and reduce the flickering of the text during a change of the text to be displayed (see col. 6, lns 62-68 of Strobel et al.).

As for claims 3 and 17, Bird et al. teach the display data signals applied to row and column electrodes by a data signal drive circuit are in the form of time dependent signals comprising pulse width modulated signals derived from an input digital video signal and representing video sample values (see Abs.). In utilizing the method of driving ICs taught by Strobel et al., these data signals can be inputted to the master IC, which in turn propagates the signals to the slave ICs.

In regard to claims 6 and 18, as cited above in claims 5 and 7, Strobel et al. teach an internal delay circuit through terminals C1 and C2, and thus is variable.

4. Claims 8-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over S-MOS System, Inc., Dot Matrix LCD Driver SED 1520/21 Version 1.0 (October, 1996) (hereinafter S-MOS) and further in view of Strobel et al. (US Patent No. 5,420,600).

Referring to claims 8 and 12, as depicted in the Dot Matrix LCD Driver SED 1520 Manual (page 7-8), a block diagram of the system and the LCD driver comprises an MPU interface for receiving plurality of input data from external microprocessor, display start line register for generating address signal from the interface circuit, a display data RAM to receive the address signal, a frame signal FR to make the LCD driver circuit generate a dual frame AC driving waveform to drive LCD, a column address counter giving column addresses of the display data RAM as shown in Fig. 2.3.8.1 (page 11 and 13), an LCD driver circuit for generating output from the display data latch circuit in combination with the FR signal (page 14). The LCD driver further comprises a selection terminal M/S input signal to select the master or slave LSI, when M/S = VDD, the driver is set master, and when M/S = VSS (page 22), the driver

is set slave. Output and input terminal is illustrated in the system block as be seen in Fig. 2.1, page 7. The input and output delay time of the FR signal can be seen from page 37, table 1 and 2.

Thus, S-MOS teaches all the limitations of claims 8 and 12, except for the display control signal is enabled when the display driver IC is set as a master by the selection terminal, and the display control signal is disabled when the display driver IC is set as a slave by the selection terminal.

However, Strobel et al. teach a chain of IC display drivers as cited above, wherein control signals are applied from outside to the internal circuit blocks via the inputs C1 and C2 (col. 14, lines 10-11). As shown in Fig. 5, terminals C1 and C2 which permit the operating mode of the IC to be selected (it is noted that 'operating mode control BAS itself is externally controlled', col. 8, lines 46-48). If a plurality of ICs are to be connected to form a chain, C1 and C2 of the master are connected to the controlling processor, cf. also FIG. 5 (control signal is enabled for master IC). On the other hand, in all the slaves C1 is constantly applied to high level and all the C2 terminals are directly connected to the C2 terminal of the master, cf. FIG. 5 (control signal is disabled for slave IC) (col. 12, lines 37-42). For example, C1=C2=0: the shift register SR1 is loaded out of the text memory TS;

C1=0; C2=1: the data are loaded by the input SIN into the shift register,

C1=1; C2=0: the data are loaded by the input SIN directly into the shift register SR1;

C1=C2=1: the input SIN is blocked (col. 12, lines 44-58). Thus, when C1 = C2 = 1, the display control signal is delayed.

In regard to claims 9 and 13, shown in the first table of page 22 is the input/output switching state configuration based on the control signal FR and the selection signal M/S for selecting master or slave state.

Referring to claims 10-11 and 14-15, with reference again to the table on page 22, section 3.2.3.2 of the manual for driver SED 1520/21, the state of the driver (master or slave) depends on both the M/S signal and FR signal. Therefore, it is implied a combinational logic function using either AND or OR circuit to connect these two signals in order to switch the state of the IC.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

02/18/2003

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600